

ABSTRACT

A first series combination of bit match circuits compares a predetermined bit position in data words that are involved in a compression operation. The first series combination compares the values in the predetermined bit position to determine if they are all a logical zero. A second series combination of bit match circuits compares the same predetermined bit position in the data words. The second series combination compares the values to determine if they are all a logical one. If either condition is true, the value of the bit is output through an output buffer. If both conditions are false, the output buffer is placed in a high impedance state to indicate an error condition exists in that bit position.